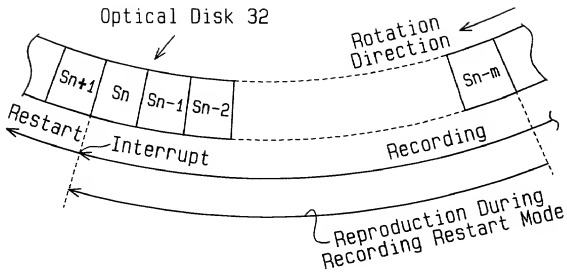
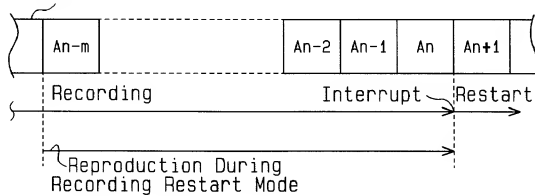


**Fig.2 (a)**

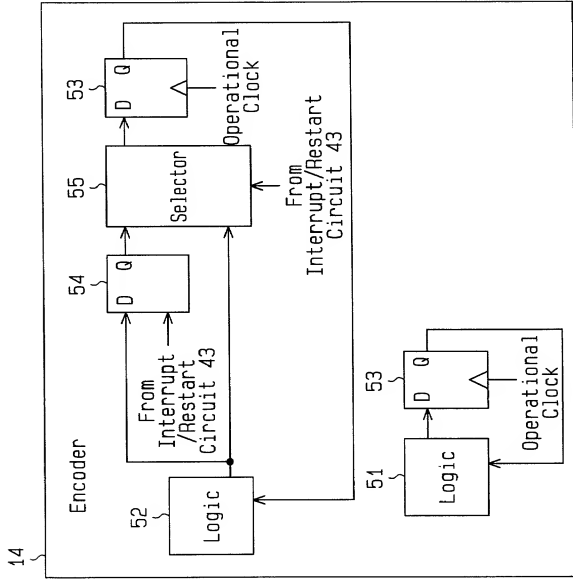


**Fig.2 (b)**

Buffer Memory 13



**Fig. 3**



The diagram illustrates a digital data recording system (1) with the following components and connections:

- Input Section (2):** A **Spindle Servo** (3) and **Spindle Motor** (2) are connected to an **Optical Head** (4).
- Head Assembly (6):** The **Optical Head** (4) is connected to a **Head Servo** (6).
- Signal Path (5):** The **Head Servo** (6) outputs an **RF Signal** (4) to an **RF Amp** (5).
- Decoder Section (7):** The **RF Amp** (5) outputs **Digital Data** (7) to a **Decoder** (7). The **Decoder** (7) includes **Subcode Decoding** (8) and **Wobble Decoder** (9).
- Control Section (10):** The **Decoder** (7) outputs a **Rotation Control Signal** (10) to an **ATIP Decoding** block (10).
- Timing and Clock Section (18):** A **Crystal Oscillation** (18) provides a **Pit Clock** to the **Decoder** (7) and a **System Clock Generation** block (41).
- Encoding and Recording Section (14):** The **System Clock Generation** (41) provides a **System Clock** (42) to an **Encoder** (14) and a **Signal Synchronization (2nd Retry) Determination** block (42). The **Encoder** (14) includes **RAM** (15) and outputs a **Subcode Synchronizing Signal** (47) to a **Location Detection** block (45). The **Encoder** (14) also receives a **Subcode** (43) from the **Signal Synchronization** block (42).
- Buffer and Interface Section (11):** The **Encoder** (14) is connected to a **Laser Drive** (16) and a **Buffer Memory** (13). The **Buffer Memory** (13) is connected to an **Interface** (11).
- Control and Management Section (19):** The **Interface** (11) is connected to a **Personal Computer** (31). The **Interface** (11) also receives a **Restant Signal** (44) from the **Location Detection** block (45). The **Interface** (11) outputs a **Restant Signal** (46) to another **Location Detection** block (46).
- Recording Control Section (20):** The **Interface** (11) outputs a **Recording Control** signal (21) to a **Recording Control** block (20). The **Recording Control** block (20) is connected to a **Buffer Underrun Determination** block (20).
- Access Control Section (19):** The **Recording Control** block (20) is connected to an **Access Control** block (19).
- System Clock Section (41):** The **System Clock Generation** block (41) provides a **Subcode Synchronizing Signal** (47) to the **Location Detection** block (45) and a **Subcode** (43) to the **Signal Synchronization** block (42).
- Signal Synchronization Section (42):** The **Signal Synchronization (2nd Retry) Determination** block (42) outputs a **Subcode** (43) to the **Encoder** (14) and a **Subcode Synchronizing Signal** (47) to the **Location Detection** block (45).
- Location Detection Section (45):** The **Location Detection** block (45) outputs a **Restant Signal** (44) to the **Interface** (11) and a **Restant Signal** (46) to another **Location Detection** block (46).
- Address Memory Section (43):** The **Address Memory** (43) is connected to the **Signal Synchronization** block (42) and the **Location Detection** block (46).
- Interrupt/Restart Section (48):** The **Interrupt/Restart** block (48) is connected to the **Address Memory** (43) and the **Location Detection** block (46).

